REMARKS

Minor amendments are made to the specification in this paper. Those amendments minor typographical errors and other errors of usage to place the specification in better condition for publication upon allowance of this application.

The application had eighteen claims pending for examination in the last Office Action. Claims 9-18 are cancelled in this paper, and new claims 19-32 are added. Claims 1-8 and 19-32 are thus now pending for examination. Reexamination and reconsideration of these claims are thus respectfully requested.

Claim 1 is directed to a semiconductor memory device that includes a memory cell on a semiconductor substrate. The memory cell includes "a floating gate" and "a control gate," with an "inter-layer insulating layer" between them. The inter-layer insulating layer includes "a silicon oxide layer contiguous to said floating gate," "a first silicon nitride layer provided by a CVD method on said silicon oxide layer," and "a second silicon nitride layer provided by a JVD method on said first silicon nitride layer and having a lower trap density than that of said first silicon nitride layer."

Claim 1 was rejected under section 112 on that ground that "a proper definition of trap density has not been provided." This rejection is respectfully traversed, because one of ordinary skill in this art at the time the invention was made would have (a) understood adequately the meaning of the term "trap density" and (b) been able, without undue experimentation, to produce a semiconductor memory device with the claimed properties.

The McGraw-Hill Dictionary of Scientific and Technical Terms (5th ed. 1994) provides the following definition for the word *trap* – "Any irregularity, such as a vacancy, in a semi-conductor at which an electron or hole in the conduction band can be caught and trapped until released by thermal agitation." For *density*, the same reference provides the following – "The total amount of a quantity, such as

energy, per unit of space." [1] *Trap density* is thus the total number of *traps* in a unit amount of a given substance – in claim 1, the second silicon nitride layer.

That those of ordinary skill in the art would have so understood *trap density* is shown by U.S. Patent No. 5,731,238, the *Cavins et al.* patent that the Examiner cites in the most recent Office Action. That reference teaches "a method of forming an integrated circuit," in which:

> A first layer of JVD silicon nitride 16 is deposited on substrate 20 so that it has a trap density of less than about 1×10^{11} traps/cm^2 and a hydrogen concentration of less than about 10 atomic percent. Both concentrations are characteristics of JVD silicon nitride and are significantly different than the concentrations found in either conventional CVD or PECVD silicon nitride. [2]

This same passage demonstrates that one of ordinary skill in the art would have had no undue difficulty forming a second (JVD) silicon nitride layer over a first (CVD) silicon oxide layer – these techniques being well understood -- and that it was also understood that the JVD layer would naturally have a trap density lower than that of the CVD layer.

Claim 1 was also rejected under section 102 or section 103 as being allegedly unpatentable over Takeuchi in view of Cavins. [3] In doing so, the Examiner explicitly declined to give any weight to the limitations specifying the particular processes (CVD vs. JVD) by which the two silicon nitride layers are made. This was based on, *e.g.*, *In re Thorpe*, 777 F.2d 695, 227 U.S.P.Q. 964 (Fed. Cir. 1985). [4] According to *Thorpe*, "The patentability of a product does not depend on its method of production. *If the product is the same as or obvious from a product of the prior*

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[1] Copies of the title page, copyright notice, and relevant definitions from this reference are attached hereto for the Examiner's convenience.

[2] *Cavins*, col. 4, lines 13-19.

[3] *Office Action*, at pp. 7-8.

[4] This approach is discussed in section 2113 of the M.P.E.P.

art, the claim is unpatentable even through the prior product was made by a different process." [5/]

The Examiner contends that "Applicant has burden of proof in such cases." [6/] This statement is at least vague, however, and potentially misleading as well. Actually, the initial burden is always on the examiner to factually support a *prima facie* case for rejection. [7/] If the Examiner makes out such a *prima facie* case, the burden then shifts to the applicant to rebut it. [8/] In claims with product-by-process limitations:

> Once the examiner provides a rationale tending to show that the claimed product appears to be the same or similar to that of the prior art, although produced by a different process, the burden shifts to applicant to come forward with evidence establishing an unobvious difference between the claimed product and the prior art product. [9/]

Claim 1 is not anticipated by Takeuchi. Takeuchi describes a memory device that includes stacked silicon oxide and silicon nitride films. Takeuchi, though, does not teach any construction in which a first CVD silicon nitride layer is provided on a silicon oxide layer, and a second JVD silicon nitride layer is provided over the first.

The Examiner alleges, though, that "the method for depositing the silicon nitride layers, *e.g.*, JVD, is an intermediate process step that *does not affect the structure of the final device.*" [10/] This assertion, which might appear reasonable enough at first glance, is actually factually incorrect. In fact, CVD-deposited silicon nitride films are, perhaps surprisingly, quite different from JVD-deposited silicon

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[5/] 777 F.2d at 695, 227 U.S.P.Q. at 966 (emphasis supplied).

[6/] *Office Action*, at page 5.

[7/] *See, e.g.*, M.P.E.P. § 2142.

[8/] *Id.*

[9/] M.P.E.P. § 2113, *citing In re Marosi*, 710 F.2d 798, 802, 218 U.S.P.Q. 289, 292 (Fed. Cir. 1983).

[10/] *Office Action*, at page 7 (emphasis supplied).

nitride films, and those differences are relevant to the inventions defined by the claims.

Evidence of these difference appears in the Cavins patent, which teaches that:

> Unlike conventional [CVD] silicon nitride films, a JVD silicon nitride film is formed without using a hydrogen-containing nitrogen source gas.
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> JVD silicon nitride films differ from conventional silicon nitride films in that they conduct current predominantly with Fowler-Nordheim tunneling rather than Frenkel-Poole conduction. The present invention takes advantage of this feature in novel semiconductor structures using a JVD silicon nitride layer in the formation of a semiconductor device. Such structures are not practical with conventional silicon nitride films due to their widely-recognized poor electrical and physical properties. [11]/

As noted above, the Cavins patent also reveals that:

> A first layer of JVD silicon nitride . . . has a trap density of less than about 1×10^{11} traps/cm^2 and a hydrogen concentration of less than about 10 atomic percent. *Both concentrations are characteristics of JVD silicon nitride and are significantly different than the concentrations found in either conventional CVD or PECVD silicon nitride.* [12]/

Claim 1 thus requires a construction that is different from anything described in Takeuchi. The product-by-process limitations are significant and can't be ignored, moreover, because the processes that form the silicon nitride layers dictate their physical properties, and those physical properties are different from

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[11]/ *Cavins*, col. 2, lines 13-23.

[12]/ *Cavins*, col. 4, lines 13-19 (emphasis supplied).

those of the structures described in Takeuchi, and significant in the context of the invention that is claimed in this application.

The Examiner recognizes that "Takeuchi does not disclose that the second silicon nitride layer has a lower trap density than that of the first silicon nitride layer." [13]/ The Examiner, though, seeks to remedy this deficiency of Takeuchi by combining Takeuchi with Cavins. The Examiner is correct that Cavins discloses use of a JVD silicon nitride layer with a trap density lower than that of a CVD silicon nitride layer.

It isn't enough, however, to identify multiple references that disclose all of a claim's limitations. A proper *prima facie* obviousness rejection requires as well that information be identified in the prior art that would have motivated one of ordinary skill in the art to make the combination the Examiner suggests. Here, the Examiner identifies the following as supplying that motivation. "It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the second silicon nitride layer of Takeuchi having a lower trap density than the conventional silicon nitride trap density in order to improve the electrical performance of the device as taught by Cavins." [14]/

The required motivation cannot be found, though, (*i.e.*, the suggested combination is improper) where the references themselves teach away from that combination. [15]/

There is no motivation in Takeuchi for using a JVD silicon nitride layer in combination with a CVD silicon nitride layer. Takeuchi does not even mention JVD

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[13]/ *Office Action*, at page 7.

[14]/ *Id.* at pages 7-8.

[15]/ *See*, M.P.E.P. § 2145, at page 2100-153; *see also In re Geisler*, 116 F.3d 1465, 1469 (Fed. Cir. 1997)("A *prima facie* case of obviousness can be rebutted if the applicant . . . can show that the art in any material respect taught away from the claimed invention")(citation omitted); *Tec Air, Inc. v. Denso Mfg. Mich. Inc.*, 192 F.3d 1353, 1360 (Fed. Cir. 1999)("A reference may be said to teach away when a person of ordinary skill, upon reading the reference, . . . would be led in a direction divergent from the path that was taken by the applicant").

for filming a silicon nitride layer. One must look entirely to Cavins, therefore, if one is to find the required motivation to combine Takeuchi with Cavins.

Cavins, though, teaches directly away from using the JVD silicon nitride layer *in combination* either with silicon oxide layers or conventional CVD silicon nitride layers. In fact, it is Cavins' primary purpose to avoid just such a combination. Cavins is quite clear about this:

> If conventional silicon nitride is used as an inter-poly dielectric material, it must be sandwiched between two layers of insulating material such as silicon dioxide. Such structures are referred to as ONO stacks. As mentioned earlier, conventional silicon nitride is susceptible to leakage currents due to Frenkel-Poole conduction. Therefore, conventional silicon nitride layers are insulated with two layers of silicon dioxide material.
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> The present invention, however, obviates the need to form these insulating layers of silicon dioxide since JVD silicon nitride conducts predominantly with Fowler-Nordheim tunneling. Thus, the present invention can be used to reduce the number of process steps required to form an inter-poly dielectric material. The elimination of two deposition steps, previously needed to form the silicon dioxide layers, will result in a significant reduction in the manufacturing cost of non-volatile memory device 11 or other capacitor structures. 16/

Does Cavins suggest that one might profitably combine a JVD silicon nitride layer with silicon oxide or CVD silicon nitride layers? To the contrary, Cavins teaches that use of the JVD silicon nitride allows one to *omit* these extra layers, and that simplicity and "a significant reduction in manufacturing cost" can be enjoyed thereby. Were one to do as the Examiner suggests, by using a JVD silicon nitride layer in combination with other insulating layers, one would then surrender the primary advantages of Cavins' method – simplicity and low cost. Cavins thus

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16/ *Cavins*, col. 3, lines 12-29.

teaches directly away from the combination the Examiner is suggesting, and therefore cannot be seen as providing the necessary motivation.

Independent claim 1 is thus patentable over the art cited against it, and the prompt allowance of that claim is therefore respectfully requested. Claims 2-4 must be similarly allowable, as those claims depend directly from claim 1.

Independent claim 5 is similar in several respects to independent claim 1. Claim 5, though, requires an inter-layer insulating layer that includes a silicon oxide layer, and a silicon nitride layer "deposited by a JVD method on said silicon oxide layer and having a lower trap density than an ordinary trap density obtained by a typical CVD condition." The Examiner rejects claim 5 on most of the same grounds as those described above in connection with claim 1, and on the additional ground that:

> The phrase "an ordinary trap density obtained by a typical CVD condition" in claims 5 and 9 is a relative term, which renders the claim indefinite. The phrase "a lower trap density than an ordinary trap density obtained by typical CVD" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. The specification does not contain any disclosure regarding an actual magnitude or range of trap density typical for silicon nitride layers obtained by CVD. [17]/

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[17]/ *Office Action*, at page 3.

This rejection is traversed. In fact one of ordinary skill in the art would understand adequately the limitation at issue. Those of skill in this art appreciate that "a silicon nitrite layer deposited by a JVD method" necessarily has "a lower trap density than an ordinary trap density obtained by a typical CVD condition." Evidence of this appears in Cavins, which describes the deposition of JVD silicon nitride having a trap density less than that of CVD silicon nitride:

> A first layer of JVD silicon nitride . . . has a trap density of less than about 1×10^{11} traps/cm^2 and a hydrogen concentration of less than about 10 atomic percent. *Both concentrations are characteristics of JVD silicon nitride and are significantly different than the concentrations found in either conventional CVD or PECVD silicon nitride.* 18/

One of ordinary skill in the art would thus be reasonably apprised of what the claim would cover, which is all the statute requires.

> That fact that claim language, including terms of degree, may not be precise, does not automatically render the claim indefinite under 35 U.S.C. 112, second paragraph. *Seattle Box. Co. v. Industrial Crating & Packing, Inc.*, 731 F.2d 818, 221 U.S.P.Q. 568 (Fed. Cir. 1984). Acceptability of the clam language depends on whether one of ordinary skill in the art would understand what is claimed, in light of the specification.
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> . . . .
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> When a term of degree is presented in a claim, first a determination is to be made as to whether the specification provides some standard for measuring that degree. *If it does not, a determination is made as to whether one of ordinary skill in the art, in*

18/ *Cavins*, col. 4, lines 13-19 (emphasis supplied).

view of the prior art and the status of the art, would be nevertheless reasonably apprised of the scope of the invention. [19]/

As with claim 1 (and as discussed above in more detail in connection with that claim), the "process limitation" of claim 5 cannot simply be ignored in comparing this claim with the prior art. The Examiner's allegation that "the method for depositing the silicon nitride layer e.g. JVD, is an intermediate process step that does not affect the structure of the final device" is factually incorrect. To the contrary, JVD deposition of the silicon nitride layer provides the lower trap density (in comparison with the conventional deposition method) that distinguishes the resulting structure over those that Takeuchi teaches.

Independent claim 5 is thus patentable over the art cited against it, as is claim 6, which depends directly from claim 5.

Independent claim 7 is similar in some respects to claims 1 and 5. Claim 7, though, requires an inter-layer insulating layer that includes a silicon oxide layer, and "a silicon nitride layer deposited by a JVD method on said silicon oxide layer and having a quantity of hydrogen content on the order of $10^{19}/cm^3$ or less."

As with claims 1 and 5, this limitation is a significant one and not one that can be simply ignored. The JVD method specified in claim 7 is not, as the Examiner contends, merely "an intermediate process step that doe not affect the structure of the final device." [20]/ To the contrary, the structure of the final device depends directly on the method used to make it, and in particular the method used to deposit the silicon nitride layer over the silicon oxide layer. The properties of a JVD method silicon nitride layer are different from those of a conventional CVD silicon nitride layer, [21]/ and those properties are significant to the proper functioning of the invention of claim 7.

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[19]/ M.P.E.P. § 2173.05(b) at page 2100-196 (emphasis supplied).

[20]/ *Office Action*, at page 7.

[21]/ *See, Cavins*, col. 4, lines 13-24.

Nor would it have been obvious to one of ordinary skill in the art to "make the silicon nitride layer of Takeuchi having a hydrogen content of $10^{19}/cm^3$ or less in order to improve the electrical performance of the device as taught by Cavins." [22]/

As discussed above in connection with claim 1, Takeuchi fails even to mention JVD for forming a silicon nitride layer. The purpose of the configuration taught by Cavins, moreover, is to achieve a simplified construction that avoids the need for multiple sandwiched layers. Cavins thus fails entirely to suggest that one should combine a silicon oxide layer with a JVD silicon nitride layer. To the contrary, Cavins teaches that such a multiple-layer construction should be avoided, and that his construction is advantageous precisely because it does so.

Independent claim 7 is thus patentable over the art cited against it, as is claim 8 which depends directly from claim 7.

Claim 9-18 are canceled in this paper, and the rejections of those claims are therefore moot.

New claims 19-32 are added in this amendment. Of them, claims 19 and 27 are independent.

Independent claim 19 requires forming "an inter-layer insulating layer having a stacked film structure with at least two film layers including a silicon oxide film layer and a silicon nitride film layer" in which "said silicon nitride film layer is formed by a JVD method." None of the art cited against the application teaches the formation of this stacked film structure, and independent claim 19 is thus patentable. The same is true of claims 20-26, all of which depend from claim 19.

New independent claim 27 requires forming "an interlayer insulating layer having a stacked film structure with at least three film layers including a silicon oxide film layer and a silicon nitride film layer" in which "said silicon nitride film layer has a concentration of hydrogen on the order of $10^{19}/cm^3$ or less. The art cited against the application fails to disclose the formation of such a stacked film

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[22]/ *Office Action*, at page 9.

structure, and independent claim 27 is thus patentable, as are claims 28-32, which depend from it.

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is invited to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6711 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

Date: August 22, 2002

By: 
Michael L. Crapenhoft
Registration No. 37,115
Attorney for Applicant

500 South Grand Avenue, Suite 1900
Los Angeles, California 90071
Phone: 213-337-6700
Fax: 213-337-6701

Version with markings to show changes made:

IN THE SPECIFICATION:

Please replace the paragraph at page 1, lines 19-25, with the following amended text:

> FIGS. 4A and 4B show sections, taken in two directions orthogonal to each other, of the memory cell structure described above. Normally in a flash memory, the control [gate] gates of [the] a plurality of memory cells are consecutively arranged and serve as word lines. FIG. 4A is the section in the direction parallel to a direction of the word line.

Please replace the two paragraphs at page 1, line 37 – page 2, line 24, with the following amended text:

> The ONO layer 5 functions to prevent electric charges accumulated in the floating gate 3 from leaking out during a writing process to the memory cell, and, because of a necessity for confining the electric charges within the floating gate 4 over a long period of time, is required to exhibit a high insulating property. In the normal flash memory, the floating gate retains electrons. In an electron accumulating state, however, a comparatively weak electric field (a self electric field) generated by the electrons is applied to the ONO layer 5.
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> [Te] The silicon oxide layer 5a, on the side of the floating gate 4, of the ONO layer 5, if a layer thickness thereof is 5 – 6 nm, works as a Fowler-Nordheim type tunnel current conductive mechanism, wherein the electric current flowing with a low electric field is extremely small.

Further, a barrier height of the silicon oxide layer 5a with respect to silicon is as high as 3.2 eV. Accordingly, if the silicon oxide layer [5] 5a has no defect and there is no electric field enhancement effect based on a two-dimensional configuration of the floating gate 4, only the silicon oxide layer 5a must be capable of sufficiently retaining the electrons for a long time. In fact, however, there exist the defect and the two-dimensional electric field enhancement effect, and hence the ONO layer is used.

Please replace the paragraph at page 3, lines 4-14, with the following amended text:

Incidentally, when the memory cell operates, and when in a state of the electrons being held by the floating gate, a positive bias is applied to the control gate 6. It is known that a large leak current flows to the silicon nitride layer through the trap level by [a] hole conduction. Accordingly, supposing that the control gate 6 is provided directly on the silicon nitride layer 5b, the holes from the control gate 6 are injected, and therefore [an] a dielectric strength is unable to be kept well. The silicon oxide layer 5c is provided upward in order to restrain the holes from being injected from the control gate 6.